Remarks

The above-referenced application has been reviewed in light of the Examiner's Office Action dated October 10, 2006. By the present amendment, Claim 21 has been amended and new Claim 37 has been added. Therefore, Claims 17-37 are currently pending in this application. The Examiner's reconsideration of the rejections is respectfully requested, particularly in view of the above amendments and the following remarks.

In accordance with the Office Action, Claims 21-24 and 32-36 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,450,421 to Joo et al., which is assigned to the same assignee as the present application. Claim 21 has been amended to correct minor errors of a generally typographical nature. The rejections are traversed.

Claim 21 recites, *inter alia,* "A system for . . . error-correcting modulated data . . . comprising means for: (a) setting a channel code . . . (b) producing demodulated data . . . and (c) performing correction of erasures and then errors of unknown location on the information data symbols produced in the step (b), using erasure locations indicated by the erasure flags having a predetermined value, wherein the step (b) of producing demodulated data comprises the steps of (b1) outputting the information data symbols if the channel code has the information data symbols corresponding to the channel data patterns; and (b2) outputting erasure symbols as the information data symbols and setting the erasure flags to the predetermined value if the channel code has no information data symbols corresponding to the channel data patterns."

Claim 21 presents in a means-plus-function format. Accordingly, the means disclosed in the specification are read into the claim. To summarize an exemplary compact disk ("CD") reading embodiment of the present specification, an EFM demodulator receives channel code symbols and demodulates each valid channel code symbol to an information data symbol. For each invalid channel code symbol, the EFM demodulator provides an arbitrary information data symbol or one that is also an erasure symbol, and further sets a first single-bit erasure flag for each invalid channel code symbol. The information data symbols and corresponding first erasure flags are sent to a buffer.

This buffer assembles a C1 word including information data symbols and their corresponding first erasure flags, and provides this C1 word to a C1 decoder. The novel C1 data decoder of the present invention begins by checking for erasures using the first single-bit erasure flags of the current C1 word, which may be efficiently OR'ed together as single-bit flags to determine whether there are any erasures present. If there are any erasures in the current C1 word, the C1 decoder proceeds to correct a correctable number of erasures. The C1 decoder then corrects a correctable number of actual errors, where the correctable number of actual errors is dependent upon the number of erasures, that is, it is reduced by one correctable actual error for every two erasures corrected.

On the other hand, if there are no first erasure flags set for the current C1 word, only then does the C1 decoder of the present invention proceed along more conventional lines to correct only actual errors of the current C1 word. If the number of

erasures and/or actual errors is too great for the C1 decoder to handle, this C1 decoder sets each information data symbol of the current C1 word to an arbitrary information data symbol or one that is also an erasure symbol, and further sets a second erasure flag for each symbol of the current C1 word. The information data symbols and their corresponding second erasure flags are provided to the buffer.

The buffer uses the symbols and second erasure flags provided by the C1 decoder to assemble a C2 word including information data symbols and their corresponding second erasure flags, and provides the C2 word to a C2 decoder. The C2 decoder of the present invention begins by correcting a correctable number of erasures, and then corrects a correctable number of actual errors, where the correctable number of actual errors is dependent upon the number of erasures. If the number of erasures and/or actual errors is too great for the C2 decoder to handle, this C2 decoder sets each information data symbol of the current C2 word to an arbitrary information data symbol or one that is also an erasure symbol. The information data symbols are provided to the buffer.

The '421 to Joo et al. is generally directed towards correcting multiple erroneous symbols in error correcting encoded data, and shows various arrangements for correcting errors in a Reed-Solomon code recovered from an optical disk. While Joo et al. may have marked some information data symbols as erasures and/or "deleted" them prior to error correction, embodiments of the presently claimed invention flag and correct such erasures of information data symbols with the first decoder (e.g., C1 or PI) prior to correcting actual errors. Joo et al. do not fairly show "A system for . . . error-

correcting modulated data . . . comprising means for: (a) setting a channel code . . . (b) producing demodulated data . . . and (c) performing correction of erasures and then errors of unknown location" as recited in amended Claim 21. That is, the references of record in this case fail to teach or suggest the correction of erasures prior to correction of actual errors as set forth in amended Claim 21. Further, the references fail to teach or suggest correction of erasures with the first or same decoder to be subsequently used for correction of actual errors as recited in new Claim 37.

Thus, treating demodulated symbol erasures as actual errors when performing a first actual error correction using a conventional C1 decoder falls short of Applicants' presently claimed invention, which performs a more efficient error-erasure correction where erasures are corrected before actual errors are corrected. Thus, the presently claimed invention offers notable improvements over the prior art by providing erasure correction followed by error correction at each decoder, and combines this with a reduced processing overhead realizable with single-bit OR'able erasure flags.

Claim 32 recites features similar to amended Claim 21. Accordingly, neither amended Claim 21 nor previously presented Claim 32 is taught or suggested by the '421 to Joo et al.

In accordance with the Office Action, Claims 17-20 and 25-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the '421 to Joo et al. These rejections are traversed on grounds substantially similar to the anticipation rejections discussed above.

Applicant does not dispute that the use of buffers is well known in the art, but submits that it was not well known to use a first buffer for "correcting up to a first maximum number of correctable erasures and then correcting a number of actual errors not to exceed one half of the first maximum number of correctable erasures reduced by one half of the number of corrected erasures, and if no erasures are detected, correcting only actual errors of the first code word" as recited in Claim 17, for example.

In addition, it was not well known to use a second buffer for "correcting up to a second maximum number of correctable erasures and then correcting a number of actual errors not to exceed one half of the second maximum number of correctable erasures reduced by one half of the number of corrected erasures, and if no erasures are detected, correcting only actual errors of the second code word" as recited in Claim 19, for example.

Claim 25 recites features similar to those of Claim 17. Accordingly, all features of Claims 17 and 25 were neither taught nor suggested by the '421 to Joo et al. in view of the Examiner's Official Notice, whether taken alone or in combination with any of the other references of record in this case.

Conclusion

Accordingly, it is respectfully submitted that independent Claims 17, 21, 25 and 32 are in condition for allowance for at least the reasons stated above. Since Claims 18-20, 22-24, 26-31 and 33-37 each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated, and for reciting additional patentable subject matter. Thus, each of Claims 17-37 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case are earnestly solicited.

Respectfully submitted,

E. Parham 1/4/07

Eric M. Parham
Registration No. 45,747
Attorney for Applicant

Correspondence Address:

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797
Phone (516) 692-8888
Fax (516) 692-8889